CHEDULURI GANESH

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CAREER OBJECTIVE

To obtain an active and dynamic position in an organization where I can use my skills that I have acquired in my educational life for my organization and self.

ACADEMIC QUALIFICATION

Course	Institution	Board/ University	Year Of Completion	Percentage/ CGPA
M. Tech (VLSI Design)	Visvesvaraya National Institute of Technology, Nagpur.	VNIT, Nagpur	2019	7.87
B. Tech (ECE)	Adarsh college of engineering ,Chebrolu,Kakinada	JNTU Kakinada	2013	74.99%
Intermediate	G. R. C. JR college, Ramachandrapuram	Board of Intermediate Education, A.P	2009	96.70 %
S.S.C	A.P.RES School, Bhupathipalem	Board of Secondary Education, A.P	2007	90.83 %

TECHNICAL SKILLS

- Programming languages : C , Verilog , VHDL
- Design Tools : **Cadence** :Virtuoso, Genus, Innovus
  Synopysis : DC, Tcad (Sentaurus)
  Xilinx : ISE, Vivado.
  Mentor Graphics: Model Sim , Calibre
  Comsol , Matlab, Ngspice,Pspice

PROJECTS:

M.Tech

- **Title :**
  COCHLEA INSPIRED RF CHANNELIZED PRESELECTOR FILTER WITH RECEIVER FRONT END FOR UWB AND ZIGBEE APPLICATIONS.

Description:

Planar manifold channelizer design where the channelizer circuit is obtained from an electrical-mechanical analogy of a cochlear model. The electrical circuit's critical characteristic are identified, including channel filter input impedance and manifold structure, and are applied to various technologies, producing several cochlea-like channelizers at frequencies ranging from 2 GHz MHz to 10.5 GHz.

Tool used :Cadence Virtuoso

Title:

Develop a Verilog based UART (Universal Asynchronous Receiver and Transmitter), and demonstrate its working on FPGA Implementation.

- **Software used :**ISE, Cad tools
- **Description :** UART transmitter controls transmission by fetching a data word in parallel format and directing the UART to transmit it in a serial format. Likewise, the Receiver must detect transmission, receive the data in serial format, strip of the start and stop bits, and store the data word in a parallel format. Since the UART is asynchronous in working, the receiver does not know when the data will come, so receiver generate local clock in order to synchronize to transmitter whenever start bit is received.

Title:

Develop a Verilog based Hamming code and demonstrate its working on FPGA Implimentation.

- **Software used :**ISE,Cad tools
- **Description :** A commonly known linear Block Code is the Hamming code. Hamming codes can detect and correct a single bit-error in a block of data. The presence and location of a single parity bit-error can be determined by analyzing parities of combinations of received bits to produce a table of parities each of which corresponds to a particular bit-error combination. This table of errors is known as the error syndrome. If all parity are correct according to this pattern, it can be concluded that there is not a single bit-error in the Messages.
- **Title:**

  RF LOW-NOISE AMPLIFIER DESIGN FOR 2.4G Hz WIRELESS ZIGBBE TRANCIEVER APPLICATION.
- **Tool used :** Virtuoso, Caliber.
- **Description :** characterization of a low noise amplifier (LNA) operating at 2.4 GHz and implemented in a 180 nm CMOS IBM technology. Inductive source degeneration topology is used, because of its good trade-off between input matching and Noise Figure. Simulation results show a gain of 17.96 dB and a Noise Figure of 2.58 dB for a power consumption of 11.7 mW. All the design steps are presented: gain optimization and bias point analysis, input and output matching, insertion of a cascode stage, stability, noise Figure analysis and layout design.

B.Tech

Title :

AUTOMATIC CAR PARKING SYSTEM

- **Description :** We designed microcontroller based automatic car parking system using Zigbee protocal. Now a days parking of vehicle is one of problem at shopping complexes specified space limitation. So we design a system, if all the parking places occupied by cars, then door of the parking is closed automatically. If parking place is there, then it allows the next vehicle.

CO - CURRICULAR ACTIVITIES:

- Delivered lecture on the Virtuoso simulator in the SMDP workshop conducted by VNIT
- Awarded third prize in the Idea presentation on MEMS Devices conducted in the GIAN workshop on BIOMEMS Design.
- Participated in GIAN WORKSHOP conducted by VNIT NAGPUR.
- Presented a paper on "SOS TRANSMITION" in E SPARX-2K12 at JNTU college of Engineering KAKINADA.
- Presented a paper on "AUTOMATED CAR" in MECHANO2 at University college of engineering Vijayanagaram (JNTUK).
- Attended a workshop on ROBOZEAL at ADARSH COLLEGE OF ENGINEERING.

EXTRA - CURRICULAR ACTIVITIES:

- Participated in the cricket, volleyball, chess , kho-kho in the Vihang 2k19, a sports event in VNIT
- Participated in CHESS event in the COLOURS2010.
- Participated in "INTER NIT KHO-KHO 2019"held at NIT Rourkela.

PERSONAL DETAILS

- Date of Birth : 09-09-1992
- Father's Name : Mr. Appa Rao
- Languages known : English and Telugu
- Hobbies : playing chess, running.
- Address : H.No:13-133
  Karrivari street, Chebrolu , Gollaprolu Mandal
  East Godavari Dt, Andhra Pradesh,
  PIN: 533449.

DECLARATION

I, hereby confirm that the information given above is true to the best of my knowledge.

Date :
Place : IITH

(CHEDULURI GANESH)