Swati Bhardwaj

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Career Objective:

To carry out research and development activities as an active member of team towards the accomplishment of the organizational goals, to achieve success in my career and prove to be an asset to the organization and the society.

Qualifications:

S.No.	Examination passed	Board/University	Year	% Marks
1.	Ph.D. (Microelectronics & VLSI)	IIT, Hyderabad	2019	8.00 (CGPA)
2.	M.Tech. (VLSI Design)	NIT, Kurukshetra	2012	8.758 (CGPA)
3.	B.E. (Electronics & Comm. Engg.)	MDU, Rohtak	2010	77.51 %
4.	Senior Secondary(XII)	CBSE	2006	77. 60 %
5.	Matriculation(X)	CBSE	2004	84.00 %

Experience:

- Research Scholar at Electrical Department, IIT Hyderabad since July 2014 to present.
- Assistant Professor , ECE Department at Sharda University, Greater Noida(July 2012 to July 2014), have been teaching VLSI related subjects to M.Tech VLSI Design students and B.Tech students (CMOS VLSI Design, Verilog, Low Power VLSI Design, Embedded System Design, Microprocessor) and Major Project and Thesis Supervisor for B.Tech students.

Publications:

Journals:

- **S. Bhardwaj** , R. Shashank, A. Acharyya, “Simplex FastICA: A Low Complex Accelerated Coordinate Rotation based nD FastICA for Real time Healthcare Applications”, *IEEE Transactions on Very Large Scale Integration*, 2018 (In Press)
- **S. Bhardwaj,** S. Mopuri and A. Acharyya, "Coordinate Rotation based Design Methodology for Square root and Division computation", *IEEE Transactions on Circuit And Systems II* , 2018
- **S. Bhardwaj**, R.Shashank, et al., “Vector Cross Product and Coordinate Rotation based nD Hybrid FastICA” , *Journal of Low Power Electronics*, Vol:14, Issue: 2, pp: 351-364, June 2018.
- **S. Bhardwaj** and A. Acharyya., “Low Complex CORDIC based SoC Architecture Design for SCICA for Protein Analysis ” , *IEEE Transactions on Very Large Scale Integration*, 2018 (Under Preparation)

- **S. Bhardwaj,** et al.,"CORDIC based Low Complexity N-D Gram-Schmidt Orthogonalization Architecture Design Methodology", *IEEE Transactions on Very Large Scale Integration*, (Under Preparation)
- **S. Bharadwaj** and A. Acharyya, "Low Complexity Single Channel ICA Architecture Design Methodology for Low Power Healthcare Applications*", VLSI Circuits and Systems Letter, IEEE Computer Society*, Vol: 3, Issue: 3, pp: 2-11, October 201**7**
- B. Adapa, D. Biswas, **S. Bhardwaj**, S. Raghuraman, A. Acharyya, and K. Maharatna. "Coordinate Rotation-Based Low Complexity K-Means Clustering Architecture." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25, no. 4 (2017): 1568-1572.

Conferences:

- Presented a research paper " Low Complexity Hardware Accelerator for *n*D FastICA based on Coordinate Rotation,", **S. Bhardwaj** , R. Shashank, A. Acharyya, *2017 IEEE International Workshop on Signal Processing Systems (SiPS), Lorient.*
- **S. Bhardwaj**, S. Raghuraman, A. Acharyya, "Coordinate Rotation and Vector Cross Product based Hardware Accelerator for *n*D FastICA" *IEEE, ECCTD, 2017.*
- Presented a research paper "Low Complexity Single Channel ICA Architecture Design Methodology for Pervasive Healthcare Applications,", **S. Bhardwaj** *et al*., *2016 IEEE International Workshop on Signal Processing Systems (SiPS)*, Dallas, TX, 2016, pp. 39-44.
- **S. Bhardwaj**, P. Jadhav, B. Adapa, A. Acharyya and G. R. Naik, "Online and automated reliable system design to remove blink and muscle artefact in EEG," *2015 37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Milan, 2015, pp. 6784-6787.

Project Undertaken:

- Ph.D. Thesis on "**Low Complexity, Low Power CORDIC based Single Channel Independent Component Analysis (SCICA) Design along with SoC implementation**", Aug 2014 till date. (under the guidance of Dr. Amit Acharya, IIT Hyderabad)
  - Designing and implementation of Pre-processing, ICA and post-processing for SCICA using a single CORDIC engine, thereby eliminating the complex arithmetic operations in each of those steps .
  - Designing and implementation of an accelerated, low complex signal separation technique for Independent component Analysis (ICA)
  - Developed a low complex simplified architecture for K_Means Clustering.
  - Development of Re-configurable Low complex CORDIC based FFT architecture tageted for SCICA applications.
  - Designing first of its kind Low Complex Architectural Design for SCICA based on CORDIC.
  - SoC design of the proposed architecture using UMC 180nm standard cell libraries and Xilinx Zynq7000 Evaluation Board .
- **High Speed** $N \times N$ **AFDX Switch Logic Implementation** Dec 2015 – June 2016 (in collaboration with RCI (DRDO), Hyderabad)
  - Designed a fully parameterized architecture in Verilog for N X N AFDX Switch.

- Prototyped the design for 4 ports on NetFPGA, and verified the switching on packets sent at 100 Mbps.
- Latencies observed were under 10 µs, on par with state-of-the-art switches.

- M.Tech Thesis on **"Programmable hardware interface design for capturing and transmitting the audio sample for disease detection using FPGA via GSM Modem**", June 2011 - May2012.
- Design a micro-programmed control unit of 16 bit CPU using Sparten3E FPGA, Feb -June 2011.
- B.Tech Major Project, Developed an Autonomous ROBO-SPY (LFR based) using 8051 Microcontroller, Jan 2010-May 2010.

Area of Interest:

- Digital VLSI Design
- Signal Processing Algorithms and VLSI Architectures
- Solutions for Biomedical Applications based on signal processing for VLSI
- ASIC Design and FPGA Prototyping
- Embedded System Design

Training and Workshops Attended:

- Attended four days workshop and conference and presented paper at IEEE International Workshop on Signal Processing Systems (SiPS), Lorient (France), 2017.
- Attended International Student Conference on VlSI Design and Embedded System, VLSID Hyderabad, 2017.
- Attended and presented paper at IEEE International Workshop on Signal Processing Systems (SiPS), Dallas (U.S.A.), 2016.
- Attended Gian course entitled "Digital Chip Design of futuristic Cardio-vascular health Monitoring, IIT Hyderabad, 2017.
- Attended ARM Technical Training Course on Cortex M0+ System Design, IIT Hyderabad, 2016.
- Attended International Conference of Indian Academy of Cerebral Palsy (IACPCON), Hyderabad, 2014.
- Six-week Training from TICO Institute of Embedded Technology, New Delhi. Practical work on Embedded System related to 8051 Microcontroller during June-July 2008.
- Six-week Training from DIAL, New Delhi during June-July 2009.

Technical Skills:

- **Programming:** Verilog, C language, TCL scripting, Assembly x85
- **EDA Tools:** Xilinx ISE and Vivado Design Suite, MATLAB, ModelSim (Mentor Graphics), Design Compiler (Synopsys), VCS simulator (Synopsys), Prime Time (Synopsys), IC Compiler (Synopsys).
- **Domain Knowledge**: ASIC/FPGA Design Flow, RTL Coding, FSM based design, Static Timing Analysis , Physical Designing, Logic Synthesis, Front-end Designing

Achievements:

Technical Activities:

- Received Certificate of Research Excellence from IIT Hyderabad in 2016, 2017,2018
- IInd position for Poster Paper Presentation at Research Scholar Day, IIT Hyderabad, 2018
- Received appreciation letter for Oral Presentation for research paper at SiPS-2016, Dallas, USA and SiPS-2017, Lorient, France
- Faculty Project Supervisor for Twenty B.Tech students 2012-2014
- Received Scholarship from MHRD, Govt. of India for two years during M.Tech
- Qualified GATE 2010, 2011, 2012, 2013, 2014 with 93.3, 92.0, 94.5, 91.8, 96.3 percentile
- IInd position in Paper presentation in SURGE 2011, NIT Kukukshetra
- Coordinator of technical society for Electronics Engineers, during national level technical fest, TECHNOVA 2009, DCRUST
- Ist position in Technical Exhibition on National Science Day, DCRUST, 2009
- 1st position in Circuit Realization, Technova, 2008
- IIIrd position in Robotics, Technova,2007
- Participated in ROBOWARS in Technova organized by D.C.R.University of Science and Technology(DCRUST), Murthal, in the years, 2008,2007& 2006.

Extra-curricular Activities:

- Anchor during various cultural activities at IIT Hyderabad, 2014-2018
- Active Member of Green Office and Photography Club, IIT Hyderabad 2015-2018
- Placement Cell Coordinator at Sharda University, 2013-2014 and NIT Kurukshetra, 2011-2012
- Anchor during national cultural fest SURGE 2011, NIT Kurukshetra
- Served as a Coordinator for Surge-11 held at NIT Kurukshetra
- IInd position in Singing, Cult Electronica, 2010
- IInd position in Case-Study, Rhythm, 2009
- Core-Committee member of LISOC (Literary society) at DCRUST, Murthal, 2009-10
- Chief Coordinator of LISOC (literary Society) for cultural fest, Rhythm 2010
- Ist position in Poster Presentation, Techno-Rhythm, 2007

Sports Activities:

- Ist position in Discus Throw and Shot Put Throw, IIT Hyderabad, 2018
- Participated in Long distance Friendship Race at IIT Hyderabad, 2014, 2015, 2017, 2018.
- Participated in Discus Throw and Shot-Put at Inter-IIT Sports Meet IIT Mumbai, 2014
- Ist position in Chess Competition, 2015, 2010, 2009
- Ist position in Discus Throw, NIT, Kurukshetra, 2012
- Ist position in 1500 meter race and 800 meter race, NIT, Kurukshetra, 2011
- IInd position in Discuss Throw Competition and Badminton Competition, 2010
- IInd position in Basketball Competition, 2010, 2008, 2007, at DCRUST, Murthal

Hobbies:

- Interested in creative activities
- Singing and Listening to Music
- Reading Mystery novels

Personal Information:

Name	:	Swati
Father's name	:	Dr. Rajender Singh
Mother's name	:	Mrs. Promila Devi
Nationality	:	Indian
Date of Birth	:	14 Nov 1988
Sex	:	Female
Language known	:	Hindi, English

Reference:

Dr.Amit Acharyya
Assoiciate Professor
Department of Electrical Engineering
Indian Institue of Technology, Hyderabad
Email: amit_acharyya@iith.ac.in

Declaration:

I here by declare that the information given above is true to the best of my knowledge.

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