Analog layout opportunities (Full-time contract basis) at IITH within the R&D project.

Number of positions: 3 no.

Key Responsibilities:

- Work on custom layout Analog IPs like PLL, ADCs, DACs, Voltage Reference Generators, High speed IOs and custom layout of standard cells
- Performing verification checks like DRC/LVS/Antenna and fixing violations
- Work closely with the design engineers and layout engineers in designing and successfully delivering Analog Layouts
- Need to work and review layouts which produces good yield
- Experience in using Cadence Virtuoso Layout Editor, Mentor Graphics Calibre verification tool (Assura and/or Hercules is plus)
- Performing various kinds of Analog Layouts, implementations from top-level floor planning down to complex block level layouts
- Knowledge of various Analog Layout Techniques
- Understanding of circuit principles as affected by layout such as speed, capacitance, power, noise and area
- Ability to exchange and communicate information with Analog Designers and the team members
- Possess good team building skills
- Excellent communication, documentation and presentation skills

Preferred Qualification:

Looking for a fresher trainee with 6 months / 1+ years of experience with education BTECH – ECE.

Salary: 10k per month.

Contract Period:

1 year and will be extended based on their performance and requirements.

Job Location: IIT Hyderabad, DARMIC LAB.

Joining Date: 1st February 2026

How to apply:

Kindly drop your latest resume at **parameshwari.p@ee.iith.ac.in** on or before 25th January 2026.

Last date to receive CV is by 25th January 2026.