Vemishetty Naresh

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Objective: To work productively in a creative and research oriented environment that results in value addition to the organization, self- satisfaction and enhancement of my skills.

Experience

Indian Institute Of Technology-HYDERABAD
Project Associate, July 2013 (3/7/2013 to 31/12/2013) .

- Responsible for the developing the SoC Architecture.
- Involved in full chip implementation of a design from Netlist to GDSII based on Internet of things (IoT) for smarter health care.
- Responsible for integration of the complete design, creating I/O Pads, Performing Synthesis and Static Timing analysis.

Academic Credentials

Degree	Institute	Year	%/CGPA
Doctor of Philosophy (PhD)	Indian Institute of Technology Hyderabad	Pursuing	9.0
M.S (By Research) (VLSI Systems)	National Institute of Technology, Tiruchirapalli	2013	8.2
B.Tech (ECE)	Aurora's Technological Research Institute, Hyderabad	2010	63.44
Class XII	SR Junior College, Warangal	2006	92.7
Class X	Holy Angles high school, Mahabubabad	2004	82

Academic Achievements

- Acceptance of Abstract at **Computing in Cardiology (CINC)** conference on "**An on-chip Robust Real-time Automated Non-invasive Cardiac Remote Health Monitoring Methodology**"
- Presented a paper on "**An area efficient multiplexer based CORDIC**" at an IEEE conference ICCCI-2013.
- Presented a paper on "**PSoC based isolated speech recognition**" at an IEEE conference ICCSP-2013.
- Presented a paper on "**CORDIC Based Universal Modulator**" at an IEEE conference RAECS – 2014

Core Competencies

CMOS fundamentals	RTL Coding	Synthesis
Static Timing Analysis	Floor plan	Power Plan

Tools Expertise

Simulation	ModelSim (Mentor Graphics), Xilinx-ISE, Incisive (Cadence).
Linting	Cadence HAL.
Formal verification	Formality (Synopsys).
Synthesis	DC Compiler (Synopsys), RTL Compiler (Cadence).
Timing Analysis	Primetime (Synopsys).
Layout	Virtuoso Xl (Cadence), IC Compiler (Synopsys).

Computer Skills and Languages

Verilog	C

Academic Projects

Project #1	**Direct Digital Frequency Synthesizer**
Tools	**Xilinx ISE, Chipscope Pro, VCS, DC compiler**
Description	The aim of the project is to generate two un-modulated carrier signals in quadrature (sint and cost) and generation of carrier with phase, frequency and amplitude modulation. The design uses CORDIC algorithm, phase accumulator and DAC. This design is done in verilog HDL and implemented in FPGA SPARTAN-3E starter kit.

Project#2	**An area efficient multiplexer based CORDIC**
Tools and Kits	**Xilinx ISE, Spartan 3E Kit**
Description	The main objective of project is to generate sine and cosine waves using CORDIC algorithm. This algorithm reduces the computation to addition, subtraction and shifts. Area occupied by the algorithm in FPGA is reduced by eliminating one adder stage and replacing further adder stages with Muxes.

Project#3	**PSoC based isolated speech recognition system**
Tools and Kits	**PSoC Creator, Cypress EDK kit**
Description	The project aims to implement isolated speech recognition system using PSoC5

	(ARM Cortex-M3) processor. Recognition performance is studied using two feature extraction techniques (Zero crossing and Zero crossing with end point detection) and minimum distance classifier.

B.Tech Project Details

Project #5	Frame Identification and PQRST extraction Methodology in ECG signal targeting Remote heath care.
Tools	**Xilinx ISE, LEDA, DC Compiler**
Description	This project deals with an on-chip realization of the architecture implemented to automate the process of identifying the perfect boundaries in a chunk of PQRST frames and extracting features (RR-interval, the QRS-length and PR-interval) of all the chunks with in the proper boundary of ECG signal. This methodology has been implemented using Discrete wavelet Transform(DWT) developed by using the concept of resource sharing making it highly low complex and provides scope in automating the cardiac health prognosis suitable for mobile devices in remote healthcare.

Extra-Curricular Activities

- NSS (National Service Scheme) volunteer from 2006 to 2008.
- Organized/volunteered various cultural festivals at NIT-Trichy.

Declaration

I hereby declare that the above mentioned information is true to the best of my knowledge and belief.

Yours Sincerely,

Vemishetty Naresh