Dr. Chandrajit Pal

Curriculum Vitae in short

"What golden deed have I done today ?" - Chandrajit Pal

Education

2017 (April) to 2019 (August). Worked as **National Post-Doctoral Fellow (DST, SERB, Govt of India)** in Department of Electrical Engineering, Indian Institute of Technology (IIT), Hyderabad, India.

2012–2017 **Ph.D. (Tech.) DST Inspire Fellow (DST, Govt of India)**, University of Calcutta, India.

2016 **Newton Bhabha Fellow**, Research Intern in School of Electronics and Computer Science, University of Southampton, England.

2008–2010 **M.Tech.**, Information Technology, University of Calcutta, India.
Percentage – 85.75, First Class First (University Topper, **GOLD MEDALIST**)

2004–2008 **B.Tech.**, Information Technology, West Bengal University of Technology, India.
Percentage – 86.8, First Class.

Post-Doctoral Project Title:

Adaptive Approximate COMPuting Systems Design for biomedical devices with machine learning.
Supervisor: Prof (Dr.) Amit Acharyya (EE dept, IIT Hyderabad, India.)

Ph.D. Thesis Dissertation:

Title: **Design and implementation of multimedia algorithms on reconfigurable architecture like FPGA**.
Supervisors Professor **Dr. Amlan Chakrabarti & Dr. Ranjan Ghosh**
Description To design and evaluate multimedia algorithms on reconfigurable platform as well as exploring the multimedia data security domain on the same reconfigurable platform as its importance is gaining day by day. With the advent of the mobile embedded multimedia devices that are required to perform a range of multimedia tasks, especially image processing tasks, the need to design efficient and high performing image processing system in a short time to market needs to be addressed. A wide range of functions (processors/controllers, application-specific modules, data storages, and mixed-signal circuits) can be combined on a single chip with the advent of the reconfigurable hardware concept. Thus, a single chip can become a high performing and inexpensive system for various multimedia applications (including image, video, graphics and audio) which play an important role in our daily lives.

Master's Thesis Dissertation

Title: **Design and implementation of FPGA based high speed data acquisition systems for embedded applications**.
Supervisor **Professor : Dr. Amlan Chakrabarti**
Description: This thesis explored the different methodologies and implementation techniques for realizing real time data communication in FPGA based systems with both analog and digital type of data as well as transmitting data through high speed gigabit ethernet connectivity.

Experience:

Industry:

1. (August) 2019 to 2021 (August) Redpine Signals Inc as **AI Research Engineer**.
2. 2021 (September) to 2022 (May) Ceremorphic Technologies India Pvt Ltd as **Senior Engineer**.

   N.B: Redpine Signals name converted to Ceremorphic Inc (which is their AI/ML unit)

Academic:

2022 May to present: **Senior Research Associate** in Electrical engineering department, IIT Hyderabad

2017-2019 **National Post-Doctoral Fellow (DST, SERB, Govt of India))** in Department of Electrical Engineering, Indian Institute of Technology (IIT), Hyderabad, India.

2016: **University of Southampton**, Hampshire, England, **Newton Bhabha Fellow**.
Efficient algorithm design and prototype hardware architecture (parallel and scalable implementation issues) for functional brain connectivity formulation from multi-channel EEG data, extract the markers for its quantitative characterization and finally for computing the temporal variability of such markers which typically conveys the implicit nature of cognitive efficiency.
Worked under the supervision of **Prof. Koushik Maharatna**.

2010–2012 **Sikkim Manipal Institute of Technology**, *Sikkim, India*, **Teaching Experience as Assistant Professor**.
One and half year teaching experience as an Assistant Professor In Sikkim Manipal Institute of Technology (a constituent college of Sikkim Manipal University of health, medical and technological sciences), Gangtok , East Sikkim-737136. After completion of M.Tech in 2010 from University of Calcutta, started working as an Assistant Professor in Sikkim Manipal Institute of Technology from 29th July 2010 to 2nd January 2012. During my teaching tenure I have supervised various final year graduate engineering projects. From 6th January 2012 joined full time research under DST Inspire scheme, Govt. of India. During my research tenure I have supervised four master degree final year major projects and have been invited in some workshops and seminars for training purposes and as invited speakers.

Subjects Taught

- Embedded system (EC-602) along with lab (EC-609).
- Microelectronics and VLSI DESIGN(EC-703) and lab(EC-707).
- Computer communication.(EC-704)

Research interest

- Multimedia processing on reconfigurable hardware.
- Computer organization architecture and reconfigurable hardware.
- Intelligent systems.
- Approximate computing
- Artificial intelligence
- Medical signal processing

Peer Reviewer for

Journals

- Signal, Image and Video Processing (Springer)
- International Journal of Electronics (Taylor and Francis)
- Defense Science Journal (DRDO, Govt of India)
- IEEE Transactions on Circuits and Systems for Video Technology.
- International Journal of Reconfigurable Computing

Awards

2010 Gold medalist in masters (M.Tech. in Information Technology), University of Calcutta.
2011 DST Inspire Fellowship Presidential Award from DST, SERB, Govt of India.
2012 VDAT 2012 Fellowship Award.
2013 VLSI Conference Fellowship award 2013, Pune, India.
2015 Newton Bhabha PhD placement award, University of Southampton, UK.
2017 ISCAS 2017 conference studentship award.
2017 NPDF (National Post Doctoral Fellowship), DST, SERB, Govt of India
2018 AMD Best Project award (Title: Modified Huffman based compression methodology for Deep Neural Network Implementation on Resource Constrained Mobile Platforms)

Recognition:

New technique may help deploy neural networks on portable devices

Got attention in newspapers as shown below:

1. https://www.thehindubusinessline.com/news/science/new-technique-may-help-deploy-neural-networks-on-portable-devices/article26051558.ece

2. http://vigyanprasar.gov.in/isw/new-technique-may-help-deploy-neural-network.html?fbclid=IwAR2XkUL24sj2JwljLIptLyQATU_Z8DE8ayY3XmYccoIXtciafb54oxg79gM

Computer skills

Basic C,java,C sharp
Intermediate html, LATEX,Microsoft Windows, Linux.
Advanced: VHDL, Verilog, Xilinx System Generator tool, MATLAB, Python, Tensorflow, Keras.

Invited Talk:

1. DRDO RCI, Hyderabad, July 2018.
2. Anurag group of Institute, JNTU 26th June 2019.
3. AKCSIT, University of Calcutta, Kolkata 6th July 2018 (acted as SDK toolkit **FPGA trainer**).
4. Electronics and communication dept, Jadavpur University, Kolkata 2015.
5. Indian Navy, New Delhi, July 2018.
6. Refresher/Induction programme on machine learning and Pattern recognition 2020, College of engineering and Technology, Bambhori, Jalgaon.
7. Invited lectures and acted as a **industry trainer** at **FDP** (Faculty Development Programme) sponsored by AICTE, JNTUA college of Engineering, Ananthapuramu, Dept of Computer science and Engineering.
   - AI and enabling technologies for IoT (12-23 Oct, 17-28 Nov 2020)

- Data Analytics and Machine Learning using R and Python (13 to 18th July, 03-08th Aug, 2020).

Publications:

Please have a look at my google scholar profile below for the list of my published manuscripts.

https://scholar.google.co.in/citations?user=qYcI37gAAAAJ&hl=en

Languages

Bengali :**Mothertongue**
English :*Conversationally fluent*
Hindi :**Basic** *Basic words and phrases only*

Interests

- listening to music - Chess
- reading - Singing
- Acting - Football

Date of birth

27th November 1986

Contact Details:

1. palchandrajit@gmail.com

mob no:

1. 9433943797

(Dr. Chandrajit Pal)