PRATIBHA VERMA

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AREAS OF INTEREST

ASIC Design, Physical Design, STA, RTL Design, Verification, Simulation, Digital Circuit Design, DFT

PROFESSIONAL SUMMARY

- **M.Tech. in VLSI Design** from **Visvesvaraya National Institute of Technology (VNIT), Nagpur** with **7.83 CGPA** out of 10.
- Good knowledge of ASIC Design flow from **RTL design to GDSII**. Hands on experience with synthesis and analysis of HDL designs including **Static Timing Analysis**.
- Hands on experience with circuit design including **schematic**, **netlist, pre and post-layout simulations** and **physical verification** with RC extraction.
- Good understanding of Verilog HDL, Python and Linux.
- Strong fundamental knowledge of MOSFET and semiconductor concepts.
- Knowledge of FPGA implantation and testing.
- Basic knowledge of DFT and ATPG Algorithm.
- Quick learner, self-motivated, hard as well as smart working and ambitious individual with a positive attitude to learn and adopt to new things.

EDUCATION

Jul'18-Jun'20	**M.Tech. | VLSI Design** *Visvesvaraya National Institute of Technology, Nagpur*	7.83/10
Jul'11-Jun'13	**M.Tech. | ECE (Wireless communications)** *UPTU, Lucknow, UP*	76.5%
Jul'06-Jun'10	**B.Tech. | Electronics and Communication** *UIET, CSJM University, Kanpur, UP*	8.98/10
Jun'04	**Class XII (Intermediate) | PCM | (U.P. Board)**	73.2%
Jun'02	**Class X (High School) | (U.P. Board)**	71.5%

PROFESSIONAL EXPERIENCE

Oct'20-Dec'20	Worked as Project Engineer in PhotoSpIMeDx Pvt. Ltd, incubated at IIT KANPUR.
Jul'19-Jun'20	Worked on tape-out (at 180nm node) for ZIGBEE protocol system, an SoC (5mm x 5mm chip) containing RF, Analog, Mixed-Signal and Digital Blocks. Complete ASIC flow was developed, and the chip was sent for tape-out under SMDP-C2SD, a Govt. of India Program.
Jul'16-Jul'18	Worked as an Assistant Professor in Dr. Ambedkar Institute of Technology for handicapped, Kanpur, U.P.
Jul'15-Jun'16	Provided private tuition to B.Tech. students. Offered solutions to various projects based on ARDUINO and MATLAB.
Jul'13-Jul'15	Worked as an Assistant Professor at Vision Institute of Technology, Kanpur, U.P.
Jul'10-Jun'11	Provided private tuition to B.Tech. students. Offered solutions to various projects based on MATLAB.

TECHNICAL SKILLS

Languages:	Verilog, Python, Basics of C
Analog/Digital Tools:	Cadence-Virtuoso, Cadence-Innovus, Cadence-LEC, Cadence-GENUS, Synopsys-DC, Synopsys-Tetramax, Synopsys-Formality, Mentor Graphics-Calibre, Mentor Graphics-QuestaSim, Xilinx ISE, Xilinx Vivado, NGSpice
Device Modeling:	Synopsys Sentaurus TCAD, COMSOL Multiphysics
FPGA Boards:	Basys3 (Artix-7)
Operating System:	Linux - CentOS/Ubuntu, Windows 7/8/10

PROJECTS

M.Tech. (VLSI)

Soil Sensing Platform for Natural Farming

Demonstrated hardware embedded soil testing prototype using *ARDUINO UNO* and sensors like *DHT11*, *pH sensor*. Simulated sensors for soil nutrient (like P, S, C) testing using *COMSOL Multiphysics*.

2019

Implementation of NOR Gate for In-Memory Computing using 6T-SRAM

Designed 6T-SRAM and implemented it as a NOR Gate. Schematic and layout were designed using *virtuoso*. DRC & LVS checks along with RC extraction were carried out using *Calibre*. Pre and post-layout simulations were performed and analyzed.

2018

Implementation of Complete RTL to GDSII Flow for 4-bit Adder

Designed a 4-bit adder using *Verilog HDL* and performed all the steps in RTL to GDSII flow such as *simulation, synthesis, LEC, PNR, Physical Verification* using SCL 180nm technology library. Tools used: *Vivado, DC, Conformal LEC, Innovus, Calibre.*

2018

Design of Calculator and Implementation on Basys3 Board.

Designed multifunctional calculator on *Vivado* using *Verilog HDL* and implemented it on *Basys3 FPGA* board.

2018

Formal Verification of 8-bit ALU

Designed an 8-bit ALU and its test-bench using *Questa® Advanced Simulator (SVA Coding).* Formal verification was carried out.

M.Tech. (Wireless)

Performance Analysis of M-ARY PSK, MSK & GMSK Modulation for IDMA Scheme

Studied the benefits of IDMA over existing technologies. Analyzed the performance of various modulation techniques for IDMA using AWGN channel with the help of *MATLAB*.

B.Tech.

Design and Implementation of FIR Filter using FAST Adders

Studied various fast adders and their features. Simulated their propagation delays using *MATLAB*, implemented them in the FIR filter design and compared the efficiency.

PUBLICATION

2013 **Pratibha Verma**, Sanjiv Mishra, M. Shukla, Ashutosh Singh , " **M-ARY PSK Modulation Technique for IDMA Scheme**", International conference on Advanced Computing Networking and Informatics "ICACNI-2013" Central Institute of Technology, Raipur, June 12-14, 2013. (**SPRINGER)**

OTHER ACTIVITIES, ACHIEVEMENTS & HONOURS

- Teaching Assistant for B.Tech. students for Device Modeling lab in VNIT, Nagpur.
- Delivered a lecture on Design Compiler, Logical Equivalence Checking and Formality in the SMDP workshop conducted by VNIT, Nagpur in December 2019.
- Volunteered in 5th International Symposium on Semiconductor Devices at VNIT, Nagpur.
- Won gold medals in shot-put, volleyball & throw-ball, bronze medals in discus throw, marathon (3km), badminton, cricket & group-dance in Vihang 2020 (Sports & Cultural Fest), VNIT Nagpur.
- Won first prize in technical paper presentation on the topic "Wi-Fi" in B.Tech. technical fest.

DECLARATION

I hereby acknowledge that the information furnished above is correct to the best of my knowledge.

Pratibha Verma.